**Assignment 4 Report**

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**Design Decisions**

In order to increase execution time for fmedian2, we implemented a data forwarding controller in our processor to replace the stall controller we had previously. We saw an improvement in execution time from 1min 6sec with stalling to 52 seconds with data forwarding. We were still above the 45 second execution goal, so our next strategy was to increase clock speed by modifying PLL. We iteratively increased clock speed and recompiled the Verliog until we started to receive negative slack messages in TimeQuest. We found 90 Mhz to be the clock speed with the most stable positive slack, so we went with that. The result was that fmedian2 executed in about 26 seconds, a huge improvement from the 52 seconds experience prior. This large increase can be attributed to nearly doubling our clock speed, which halved execution time.

We then implemented I/O devices. For HEX and LEDR, adding load functionality was simple. I made store also store to a data register as well as the displays. Then, I simply added a ternary statement in the data bus to check if a MMIO load word request was being made to either HEX or LEDR, and then simply returned the value from that data register.

**Problems/Issues**

**Contribution: 50%**

I implemented the I/O devices and timer as specified in the lecture slides, and I wrote half of the assembly for xmax.asm